GATE-ALL-AROUND 3D TRANSISTOR ON NANOWIRES FOR ULTIMATE NANOELECTRONICS

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Nanodevices based nanowires (NWs) have been identified as a potential candidate for sub-10nm technology era because of their suitability for gate-all-around (GAA) architecture which represents the ideal case for the electrostatic control and can ensure the further reduction of the “ultimate” transistor size . However, it is essential to implement these transistors on NW arrays in order to reach sufficient drive current level. In that context, vertical integration is a particularly attractive approach because of its 3-D character, which is more favorable to scale the contacted gate pitch i.e. scaling of the gate length and contact area. The vertical NW array based transistor is much easier to manufacture, because the gate length is simply defined by the thickness of the deposited gate material. Here, we present such 3D architectures with significant demonstrations both in processing (layer engineering at nanoscale), in electrical properties (high electrostatic control, low defect level).

Short CV

Guilhem Larrieu received the B.Sc. degree in material science and the Ph.D. degree in electronics from the University of Lille, Villeneuve d’Ascq, France, in 2000 and 2004, respectively. In 2005, he was a Postdoctoral Fellow with the University of Texas, Arlington. At the end of 2005, he was hired by a laboratory at the Institute for Electronics, Microelectronics and Nanotechnology, Centre National de la Recherche Scientifique (CNRS), Lille, France, as a Senior Independent Scientist (CR CNRS), working on dopant segregation technology for metallic source/drain field-effect transistors. Finally, in 2010, he moved to the Laboratory for Analysis and Architecture of Systems, CNRS, Université de Toulouse, Toulouse, France where he established a new research axis on nanowire arrays for electronics and sensing applications, which includes silicon- and III–V-based nanostructures and nanodevices ranging from the material investigation (chemical/ physical properties) to the processing, integration, and characterization of the related devices.

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